Testing Thermal Neutron-Induced Soft Errors in Semiconductor Materials

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Introduction

Soft errors are transient circuit errors caused due to excess charge carriers induced primarily by external radiation. Radiation directly or indirectly induces localized ionization that can flip the internal values of the memory cells. Our current work tries to characterize the soft error susceptibility for different memory chips working at different technology nodes and operating voltages.

Background and Related Work

Advances in very-large-scale integration technology have ensured the availability of high performance electronics for a variety of applications. The applications include consumer electronics like cellular phones and HDTVs, automotive electronics like those used in drive-by-wire vehicles, and million dollar servers used for storing and processing sensitive and critical data. These varied applications require not only higher throughput but also dependability. Even if a microprocessor is shipped without any design errors or manufacturing defects, unstable environmental conditions can generate temporary hardware failures. These failures, called *transient faults*, cause the processor to malfunction during operation time. The major sources of transient faults are electromagnetic interference, power jitter, alpha particles, and cosmic rays. Studies [1,2] have shown that a vast majority of detected errors originate from transient faults. Even a single-bit error may eventually lead to a computation failure. Therefore, managing the soft errors is a critical problem to solve in fully realizing dependable computing.

Soft error rate (SER) testing of devices has been performed for both neutron and alpha particles. Target 4 Flight Path 30L at the Los Alamos National Laboratory Neutron Science Center is a JEDEC prescribed test beam for soft errors, and is the only one of its kind. This beam is highly stable and it closely replicates the energy spectrum of terrestrial neutrons in the 2-800 MeV range while providing a very high neutron flux [3]. SER testing reported in the literature has been performed at this facility [4,5]. However, the beam availability is limited, necessitating the testing and use of alternate facilities for irradiations of these materials. Alternatively in the past, experiments were carried out with alpha particles originating from ^{238}Th foils on 0.25 μm-generation SRAMs [6]. While the elimination of borophosphosilicate glass and ^{10}B from the process flow in the 180-nm generation of SRAMs has made the low-energy neutron SER negligible [7], the behavior of thermal neutrons interacting with ^{10}B is interesting for other applications, such as using these types of materials as neutron detectors.

This study intends to observe the effect of ^{10}B and thermal neutrons on soft error rates using a thermal neutron beam at a university research reactor.

Experimental Setup and Results

The Penn State Breazeale Nuclear Reactor (PSBR) was used as the neutron source in the experiments. The

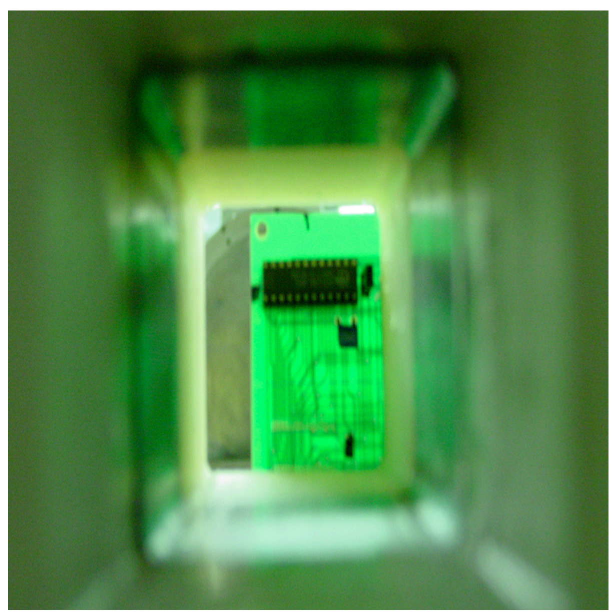

FIGURE 1: The experimental test chip, as seen through the narrow opening in the polyethylene/lead shield.

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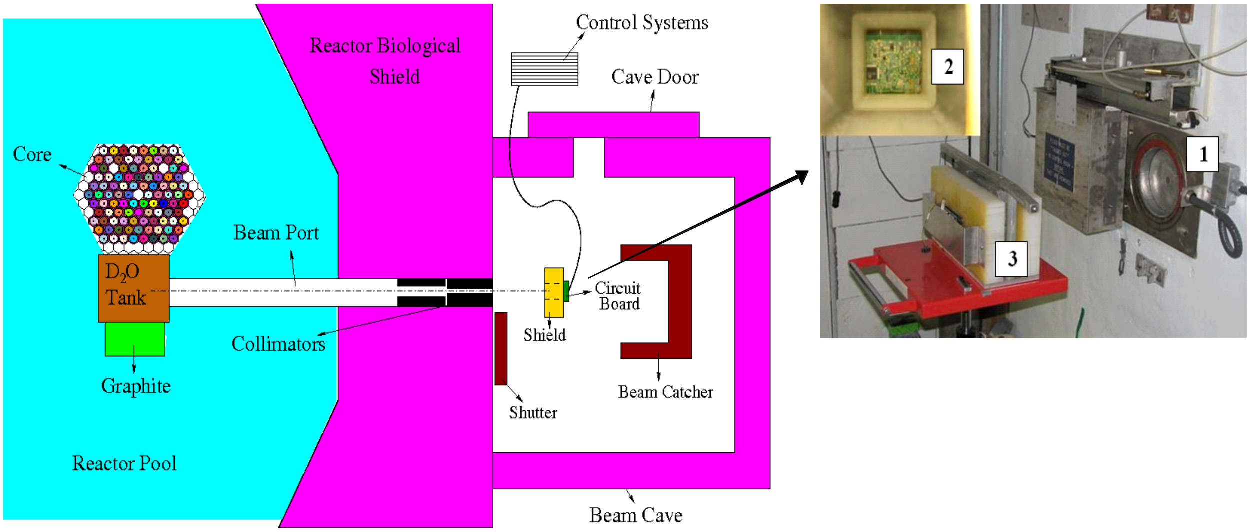

FIGURE 2: Please use this formatting for figure captions. Please make sure that figures are sized appropriately for the column width and that any text in the figure is the same size or larger than the font in the body of the summary. The RSEC book will be printed in color, so graphs and photographs may be in full color.

maximum rated power of the reactor is 1 MW in the continuous mode, and 2000 MW in the pulse mode. The reactor power is adjusted from 10 W to 1 MW to observe the SER dependence on neutron flux. No pulse-mode operation was performed. Figures 1 and 2 show the test chip and the experimental setup.

For the PSBR beam port that was used in the experiments, the beam tube looks at a D_2O tank that is positioned next to the reactor core to obtain a well-thermalized neutron beam. The average thermal neutron flux at the exit of the beam port is about 3×10^7 neutrons/cm^{2}sec. The high neutron flux (as compared to typical cosmic neutron flux values) allows for accelerated testing of the phenomenon.

The experimental setup consists of a custom board interfaced with a computer through a GPIB card (from National Instruments). The board itself has off-the-shelf SRAM memory chips. The board is controlled through a LabVIEW interface. The controlling application consists of simple routines to read and write a user specified value across the whole memory. During the readout, it compares the written value to the value in each address. The circuit board is secured in the beam cave, and connected to a PC outside using a 25-ft cable. This configuration allowed for continuous read-write, and for changing the operating conditions without interrupting the experiment.

The selected section of the board is tested on-line multiple times in the actual setup before the reactor is started. The board is exposed to the neutron flux after the reactor reaches a stable power level.

Results and Discussion

The setup described in this report allows for accelerated testing of semiconductor memory devices with thermal neutrons. The experiments and analyses have been performed only on soft errors due to thermal neutrons. Currently, a 16-kbit memory chip from Vendor A and a 4-Mbit memory chip from Vendor B were tested at various supply voltages and reactor power levels. The chip from Vendor A is rated to operate at 5 V, but was found to operate as low as 3 V. Figure 3a shows the effect of changing the supply voltage on registered soft errors in one hour. A more salient behavior can be observed with the chip from Vendor B, which was known to be denser (4-Mbits compared to 16-kbits) and was expected to have higher soft error vulnerability. Figure 3b shows the increased effect of supply voltage change on measured soft errors in this denser chip in one hour.

As shown in Equation 1, the soft error rate is expected to depend on the $Q_{critical}$ and hence on the operating voltage.

$$SER = \Phi_{th} \cdot CS \cdot e^{\left(-Q_{critical}/Q_s\right)} \qquad (1)$$

where Φ_{th} is the intensity of neutron flux, CS is the area of cross section of the node, Q_s is the charge collection efficiency, $Q_{critical}$ is the charge that is stored at the node and hence is equal to VDD * C_{node}, where VDD is the supply voltage and C_{node} is the nodal capacitance. Figures 3a and 3b confirm the exponential dependence of the SER on the device operating voltage, as well as other specifications of the device as pointed out previously by several authors [6].

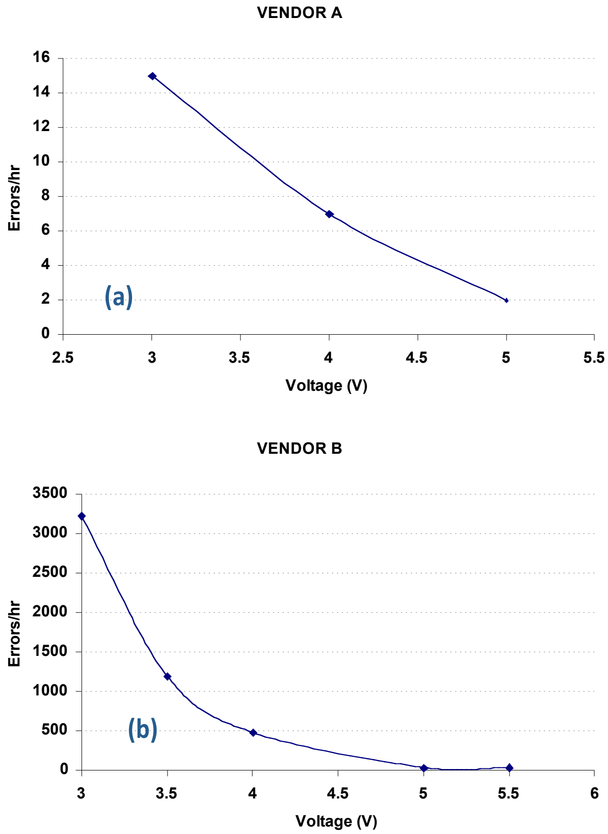

FIGURE 3: The effect of supply voltage on soft errors in (a) a 16-kbit memory chip from Vendor A and (b) a 4-Mbit chip from Vendor B

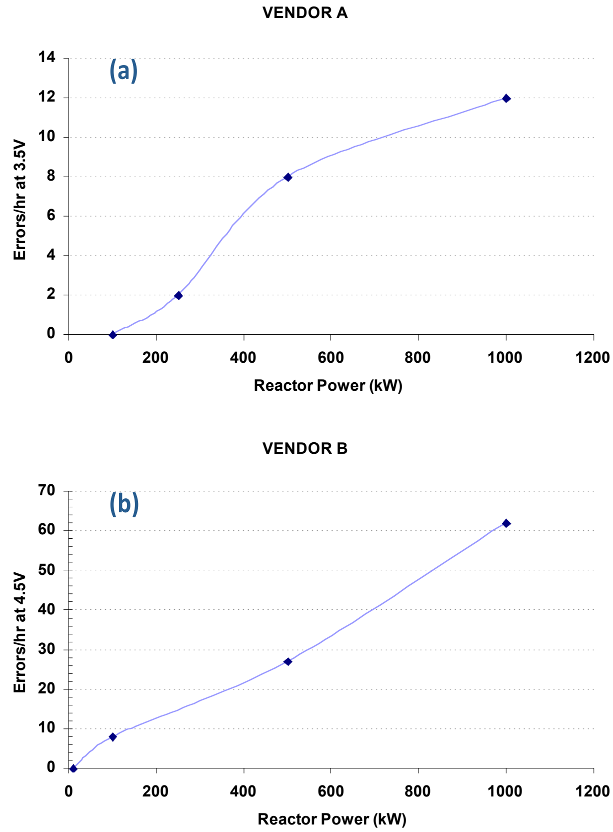

FIGURE 4: The effect of thermal neutron flux on the SER for (a) a 16-kbit memory chip from Vendor A and (b) a 4-Mbit chip from Vendor B

While employing voltage scaling for power reduction, there is a reduction in the $Q_{critical}$ of the cell. Now, if all the other factors remained the same there should be a super-linear increase in the SER. However, based on Figure 3, we see a linear increase in the SER for a corresponding decrease in the voltage. This is because for a change in supply voltage, the resultant current transient also changes. As the supply voltage reduces, the magnitude of the current changes. This affects the regenerative feedback of the SRAM cell. Thus, the soft error rate is inversely proportional to the supply voltage.

For examining the statistical accuracy of the accelerated tests, the tests were performed at various reactor power levels. Since the reactor power and the neutron flux at the exit of the beam port are directly correlated, changing the reactor power effectively changes the neutron flux impinging on the test sample, and hence is expected to increase the soft error rate. The results are presented in Figure 4.

Both figures prove that the soft error rate increases as the reactor power increases. That the soft error rate for the chip from Vendor A is not as linear as the chip from Vendor B is attributed to the relatively small size of the first chip. Hence, for statistical accuracy of accelerated soft error rate measurements, it is suggested that the measurements be performed using high capacity chips.

Future Work

This report briefly summarizes the first phase of the study that focused only on the effect of ^{10}B fission caused by thermal neutron absorption on soft error rate. The elimination of a BPSG layer in new device technologies and considerable reduction of ^{10}B content in the p-dopant significantly dropped the contribution of boron fission as a source of soft error. Therefore, for younger-generation technologies, one needs to take into account the high-energy neutron impact on device operation for proper soft error rate analysis.

The experiments will be carried out with different chips and the required coupling with the Soft Error Analysis Toolset (SEAT) will be studied in a later phase.

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